1. (Currently Amended) An integrated circuit structure utilizing fin-type field effect transistors (FinFETs) comprising:

a first FinFET having a first fin;

a second FinFET having a second fin running parallel to said first fin, wherein said first FinFET comprises a separate transistor from said second FinFET; and

an insulator fin positioned between said first fin and said second fin, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin.

2. (Original) The integrated circuit structure in claim 1, further comprising a common gate formed over channel regions of said first FinFET and said second FinFET.

3. (Previously Presented) An integrated circuit structure utilizing fin-type field effect transistors (FinFETs) comprising:

a first FinFET having a first fin;

a second FinFET having a second fin running parallel to said first fin;

an insulator fin positioned between source/drain regions of said first FinFET and said second FinFET, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin; and

a common gate formed over channel regions of said first FinFET and said second FinFET,

wherein said common gate includes a first impurity doping region adjacent said first FinFET and a second impurity doping region adjacent said second FinFET.

4. (Original) The integrated circuit structure in claim 3, wherein differences between said first impurity doping region and said second impurity doping region provide said common gate

with different work functions related to differences between said first FinFET and said second FinFET.

5. (Original) The integrated circuit structure in claim 1, wherein said first fin and said second fin have approximately the same width.

6. (Currently Amended) An integrated circuit structure utilizing complementary fin-type field effect transistors (FinFETs) comprising:

a first-type of FinFET having a first fin;

a second-type of FinFET having a second fin running parallel to said first fin, wherein said first FinFET comprises a separate transistor from said second FinFET;

an insulator fin positioned between said first fin and said second fin, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first–type FinFET and said second-type FinFET is approximately equal to the width of one fin,

a common gate formed over channel regions of said first-type of FinFET and said second-type of FinFET.

7. (Previously Presented) An integrated circuit structure utilizing complementary fin-type field effect transistors (FinFETs) comprising:

a first-type of FinFET having a first fin;

a second-type of FinFET having a second fin running parallel to said first fin;

an insulator fin positioned between source and drain regions of said first first-type of FinFET and said second-type of FinFET, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first-type of FinFET and said second-type of FinFET is approximately equal to the width of one fin; and

a common gate formed over channel regions of said first-type of FinFET and said second-

type of FinFET,

wherein said common gate includes a first impurity doping region adjacent said first-type of FinFET and a second impurity doping region adjacent said second-type of FinFET.

8. (Previously Presented) The integrated circuit structure in claim 7, wherein differences between said first impurity doping region and said second impurity doping region provide said common gate with different work functions related to differences between said first-type of FinFET and said second-type of FinFET.

9. (Original) The integrated circuit structure in claim 6, wherein said first fin and said second fin have approximately the same width.

10-33 (Canceled).

34. (Previously Presented) The integrated circuit structure in claim 1, further comprising source and drain contacts connected to ends of said first fin and said second fin, wherein source and drain contacts of said first FinFET are electrically separated from source and drain contacts of said second FinFET.

35. (Previously Presented) The integrated circuit structure in claim 6, further comprising source and drain contacts connected to ends of said first fin and said second fin, wherein source and drain contacts of said first-type of FinFET are electrically separated from source and drain contacts of said second-type of FinFET.

36. (Previously Presented) The integrated circuit structure in claim 6, wherein said first-type of FinFET is complementary to said second-type of FinFET.

37. (Currently Amended) An integrated circuit structure utilizing fin-type field effect

transistors (FinFETs) comprising:

a first FinFET having a first fin;

a second FinFET having a second fin running parallel to said first fin, wherein said first FinFET comprises a separate transistor from said second FinFET;

an insulator fin positioned between said first fin and said second fin, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin, and

source and drain contacts connected to ends of said first fin and said second fin, wherein source and drain contacts of said first FinFET are electrically separated from source and drain contacts of said second FinFET.

38. (Previously Presented) The integrated circuit structure in claim 37, wherein said first fin and said second fin have approximately the same width.

39. (Previously Presented) The integrated circuit structure in claim 37, wherein said first FinFET comprises a complementary type of transistor with respect to said second FinFET.

40. (Previously Presented) The integrated circuit structure in claim 39, further comprising a common gate formed over channel regions of said first FinFET and said second FinFET.

41. (Previously Presented) The integrated circuit structure in claim 40, wherein said common gate includes a first impurity doping region adjacent said first FinFET and a second impurity doping region adjacent said second FinFET.

42. (Previously Presented) The integrated circuit structure in claim 41, wherein differences between said first impurity doping region and said second impurity doping region provide said common gate with different work functions related to differences between said first FinFET and

said second FinFET.